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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,662	07/27/2004	Jui-Tsen Huang	12336-US-PA	4661

31561 7590 05/17/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,662	HUANG, JUI-TSEN	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed 11/4/05 has been entered. Examiner acknowledges newly admitted claims 19 and 20 which have also been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-14 and 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Abercrombie et al (5,798,568).

2. Regarding claim 1, Abercrombie et al discloses a stress relieving method for a wafer, comprising the steps of: providing a wafer (Figure 3, reference 11) with a dielectric layer thereon (Figure 3, reference 14), wherein the wafer is divided into a first area (Figure 3, reference 11) and a second area (Figure 3, references 12 and 13) such that at least no circuits are formed on the dielectric layer within the first area; forming a plurality of first openings in the dielectric layer within the first area (Figure 3, reference 14; column 2, lines 50-51); and forming a first material layer over the wafer (Figure 3, reference 15), wherein the upper surface of the first material layer has pits at locations over the first openings (Figure 3, references 31 and 32).

3. Regarding claim 2, Abercrombie et al discloses wherein the first area comprises a scribe line (column 1, lines 56-67 thru column 2, lines 1-18).

4. Regarding claim 3, Abercrombie et al discloses wherein the second area comprises a region for forming a die (Figure 3, references 12 and 13).

5. Regarding claim 4, Abercrombie et al discloses wherein the first area comprises a scribe line (column 1, lines 56-67 thru column 2, lines 1-18).

6. Regarding claim 5, Abercrombie et al discloses wherein the first area and the second area are both regions for forming a die (Figure 3, references 11-13).

7. Regarding claim 6, Abercrombie et al discloses wherein the step of forming first openings in the dielectric layer within the first area further comprises forming a plurality of second openings in the first dielectric layer within the second area at the same time and then depositing material into the second openings to form a plurality of second material layers (column 2, lines 50-51; Figure 3, reference 15).

8. Regarding claim 8, Abercrombie et al discloses wherein the first opening exposes a film layer underneath the dielectric layer (Figure 3, reference 14).

9. Regarding claim 9, Abercrombie et al discloses wherein the layer is fabricated from a dielectric material first material or a metal material (Figure 3, reference 15; column 2, lines 57-60).

10. Regarding claim 10, Abercrombie et al discloses a stress relieving method for a wafer, comprising the steps of: providing a wafer (Figure 3, reference 11) with a dielectric layer thereon (Figure 3, reference 14), wherein the wafer is divided into a first area (Figure 3, reference 11) and a second area such that no circuits are formed within the first area (Figure 3, references 12 and 13); forming a first material layer over the wafer (Figure 3, reference 15); and removing a portion of the first material layer within the first area to form a plurality of first openings (Figure 1, reference 16).

11. Regarding claim 11, Abercrombie et al discloses wherein the first area comprises a scribe line (column 1, lines 56-67 thru column 2, lines 1-18).

12. Regarding claim 12, Abercrombie et al discloses wherein the second area comprises a region for forming a die (Figure 3, references 12 and 13).

13. Regarding claim 13, Abercrombie et al discloses wherein the first area comprises a scribe line (column 1, lines 56-67 thru column 2, lines 1-18).

14. Regarding claim 14, Abercrombie et al discloses wherein the first area and the second area are both regions for forming a die (Figure 3, references 11-13).

15. Regarding claim 16, Abercrombie et al discloses wherein the first opening exposes the dielectric layer (Figure 3, reference 14).

16. Regarding claim 17, Abercrombie et al discloses wherein before forming the second dielectric layer over the wafer (Figure 3, reference 20), further comprises: forming a plurality of second openings in the dielectric layer within the second area (Figure 3, references 31 and 32); and depositing material into the second openings to form a material layers (Figure 4, reference 40).

17. Regarding claim 18, Abercrombie et al discloses wherein the first material layer is fabricated from a dielectric material or a metal material (Figure 3, reference 15; column 2, lines 57-60).

18. Regarding claims 19 and 20 Abercrombie et al discloses wherein the first material layer is a high stress dielectric layer (Figure 3, reference 14; column 2, lines 43-51)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abercrombie et al (5,798,568) in view of Sugahara (5,401,683).

19. Abercrombie et al discloses all above claimed subject matter except wherein the first opening is not deep enough to expose the film layer beneath the dielectric layer (claims 7 and 15).

Sugahara discloses wherein the first opening is not deep enough to expose the film layer beneath the dielectric layer (Figure 3A, references 354, 356 and 358).

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Abercrombie et al with the teachings of Sugahara for the purpose of forming a multi-layered semiconductor substrate.

Response to Arguments

20. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
May 14, 2006

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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